CLAIMS

What is claimed is:

1. A method comprising:

reading a file containing user-defined triggering logic used to detect one or more triggering events, the triggering logic described in a hardware description language (HDL);

inserting and connecting the user-defined triggering logic to a circuit described in HDL; and

compiling the HDL description of the circuit that includes the user-defined triggering logic.

2. The method of claim 1, wherein compiling the HDL description of the circuit comprises compiling the HDL description of the circuit to generate a register transfer level (RTL) netlist.

3. The method of claim 2, further comprising mapping the RTL netlist to a selected technology architecture.

4. The method of claim 3, further comprising performing a place and route operation to implement the circuit in the selected technology architecture.

5. The method of claim 4, further comprising programming the RTL netlist into a programmable hardware device.

6. The method of claim 5, further comprising debugging the circuit on the programmable hardware device via a debugger.

7. The method of claim 1, wherein the triggering logic has a predetermined interface.

8. The method of claim 7, wherein the predetermined interface includes a clock signal input.

9. The method of claim 7, wherein the predetermined interface includes one or more data signal inputs.

10. The method of claim 7, wherein the predetermined interface includes one or more control signal inputs.

11. The method of claim 10, wherein the one or more control signals are programmable via a debugger.

12. The method of claim 7, wherein the predetermined interface includes one or more outputs to indicate whether the triggering logic has detected a triggering event.

13. The method of claim 1, wherein the triggering logic described in HDL is written by a user and a name of the file is specified by the user.

14. The method of claim 13, wherein the user further specifies a name of a top level triggering logic block defined in the file to be connected to the circuit.

15. An article of manufacture comprising:

a machine accessible medium including content that when accessed by a machine causes the machine to perform operations comprising:

reading a file containing user-defined triggering logic used to detect one or more triggering events, the triggering logic described in a hardware description language (HDL);

inserting and connecting the triggering logic to a circuit described in HDL; and

compiling the HDL description of the circuit, including the user-defined triggering logic, to generate a register transfer level (RTL) netlist.

16. The article of manufacture of claim 15, wherein the machine-accessible medium further includes content that causes the machine to perform operations comprising mapping the RTL netlist to a selected technology architecture.

17. The article of manufacture of claim 16, wherein the machine-accessible medium further includes content that causes the machine to perform operations comprising performing a place and route operation to implement the circuit in the selected technology architecture.

18. The article of manufacture of claim 17, wherein the machine-accessible medium further includes content that causes the machine to perform operations comprising programming the RTL netlist into a programmable hardware device.

19. A computer system comprising:

a bus;

a data storage device coupled to the bus; and

a processor coupled to the data storage device, the processor operable to receive instructions which, when executed by the processor, cause the processor to perform a method comprising:

reading a file containing user-defined triggering logic used to detect one or more triggering events, the triggering logic described in a hardware description language (HDL);

inserting and connecting the triggering logic to a circuit described in HDL; and

compiling the HDL description of the circuit, including the user-defined triggering logic, to generate a register transfer level (RTL) netlist.

20. The computer system of claim 19, wherein the method further comprises mapping the RTL netlist to a selected technology architecture.

21. The computer system of claim 20, wherein the method further comprises performing a place and route operation to implement the circuit in the selected technology architecture.

22. The computer system of claim 21, wherein the method further comprises programming the RTL netlist into a programmable hardware device.